fourth pin patterns M13 and M14 may be provided or generated in the second interconnection layout (in S124). The first and second pin patterns M11 and M12 and/or the third and fourth pin patterns M13 and M14 may be formed using one of the methods previously described with reference to FIGS. 6C, 8C, and 9D. Accordingly, it is possible to provide the first and second pin patterns M11 and M12 and the third and fourth pin patterns M13 and M14, whose sizes and dispositions are different from each other, in the same standard cell layouts (e.g., the first and second standard cell layouts STD1 and STD2).

[0119] On the contrary, if the pin patterns were newly generated after the step of laying out the standard cell layout and establishing a routing structure therefor (e.g., see FIG. 4B or FIG. 5B), the same standard cell layouts may have the same pin patterns (e.g., having the same size and the same arrangement), regardless of whether there is a difference in the routing step. By contrast, in the layout design method according to some examples of the inventive concept, although the standard cell layouts are the same, it is possible to realize pin patterns for the standard cell layouts, respectively, that are different from each other in terms of their size and relative position. This makes it possible to realize a semiconductor device with optimized characteristics.

[0120] According to some examples of the inventive concept, a method of designing a layout of a semiconductor device may include laying out pin patterns in an interconnection layout of a standard cell layout, based on hitting information obtained after a routing step. Accordingly, it is possible to maximize the degree of freedom in the routing and realize a semiconductor device with high operation speed and low power consumption characteristics.

[0121] Finally, although examples of the inventive concepts have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made thereto without departing from the spirit and scope of the inventive concept as defined by the attached claims.

1. A method of producing a layout of a semiconductor device, comprising:

providing a standard cell layout, the providing of the standard cell layout comprising creating a preliminary pin pattern of an interconnection layout of the standard cell layout;

performing a routing step to produce a high-level interconnection layout in which a the preliminary pin pattern is connected to a high-level interconnection pattern; and

generating a postliminary pin pattern in a region of the interconnection layout of the standard cell layout, based on hitting information obtained upon the completion of the routing step,

wherein the postliminary pin pattern is smaller than the preliminary pin pattern.

2. The method of claim **1**, wherein the generating of the postliminary pin pattern places the postliminary pin pattern in a region that was occupied by the preliminary pin pattern such that the postliminary pin pattern and the preliminary pin pattern occupy overlapping regions in the method of producing the layout.

3. The method of claim **1**, wherein the providing of the standard cell layout comprises:

providing a logic layout including logic transistors; and

laying out a lower via pattern to connect the logic layout to the preliminary pin pattern.

4-7. (canceled)

8. The method of claim **1**, wherein the laying out of the preliminary pin pattern comprises laying out ghost patterns, in which pin information for the routing step is contained, and

the generating of the postliminary pin pattern comprises converting one of the ghost patterns that hits the high-level interconnection layout into the postliminary pin pattern.

9. (canceled)

10. The method of claim **1**, wherein the generating of the postliminary pin pattern comprises preserving a first region of the preliminary pin pattern while removing a second region of the preliminary pin pattern, and

the first region comprises a first hitting region to be connected to the high-level interconnection layout.

11. (canceled)

12. The method of claim **1**, further comprising providing a plurality of cell layouts, each based on the standard cell layout,

wherein the cell layouts have different interconnection layouts from one another, and

the generating of the postliminary pin pattern comprises replacing the standard cell layout with one of the cell layouts, based on the hitting information.

13. (canceled)

14. The method of claim **1**, further comprises laying out multiple ones of the standard cell layout, before the routing step.

15. (canceled)

16. A method of designing a layout of a semiconductor device, comprising:

providing a first standard cell layout and a second standard cell layout in a cell library, the providing of the first and second standard cell layouts comprising laying out a first preliminary pin pattern and a second preliminary pin pattern on the first and second standard cell layouts, respectively;

laying out the first and second standard cell layouts;

performing a routing step to connect the first and second preliminary pin patterns to high-level interconnection layouts; and

generating a first pin pattern and a second pin pattern using the first and second preliminary pin patterns, respectively, based on hitting information to be obtained after the routing step,

wherein the first and second preliminary pin patterns are the same as each other in terms of size and arrangement, and

the first and second pin patterns are different from each other in terms of size and arrangement.

17. The method of claim **16**, wherein each of the first and second standard cell layouts comprises the same logic layout with the same circuit.

18. The method of claim **16**, wherein each of the first and second pin patterns is smaller in size than each of the first and second preliminary pin patterns.

19. The method of claim **16**, wherein the hitting information on the first standard cell layout is different from that on the second standard cell layout.